

Bits represented:

1 1 0 0 1 0

Signal transmitted:



Fig. 1a

Bits represented:

1 1 0 0 1 0

Signal transmitted:

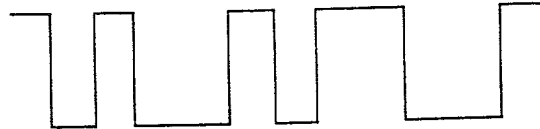


Fig. 1b

Bits represented:

1 1 0 0 1 0

Signal transmitted:

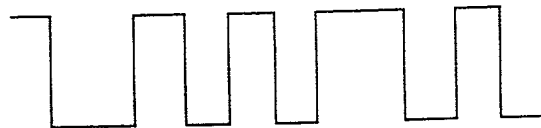


Fig. 1c

Bits represented:

1 1 0 0 1 0

Signal transmitted:

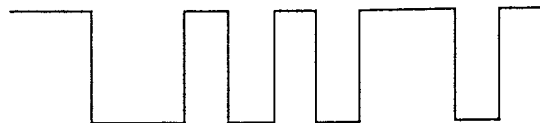


Fig. 2

0570430-070904

03760139.020901

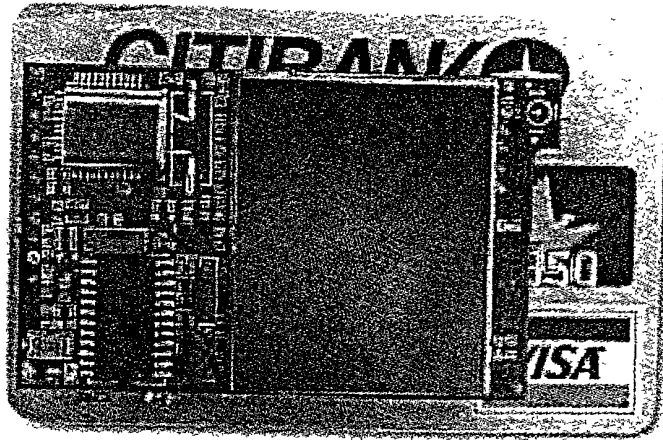


Fig. 3

J1 PIN DESCRIPTIONS

J1-1	CTS	Clear to send flow control (output)
J1-2	INT1	Interrupt line to radio processor (input, not currently implemented)
J1-3	TX	Asynchronous data output (data going from radio to user)
J1-4	RX	Asynchronous data input (data going from user to radio)
J1-5	RTS	Ready to send flow control (input, not currently implemented)
J1-6	*RESET	Reset line to radio processor (assert low to reset radio processor)
J1-7	MOSI	SPI data in (input, not currently implemented)
J1-8	MISO	SPI data out (output, not currently implemented)
J1-9	SCK	SPI data clock (input/output, not currently implemented)
J1-10	Power	+5 volts DC. (55mA in RX mode, 200mA in TX mode)
J1-11	Ground	

J2 PIN DESCRIPTIONS

J2-1	Ground
J2-2	Ground
J2-3	Ground
J2-4	Ground

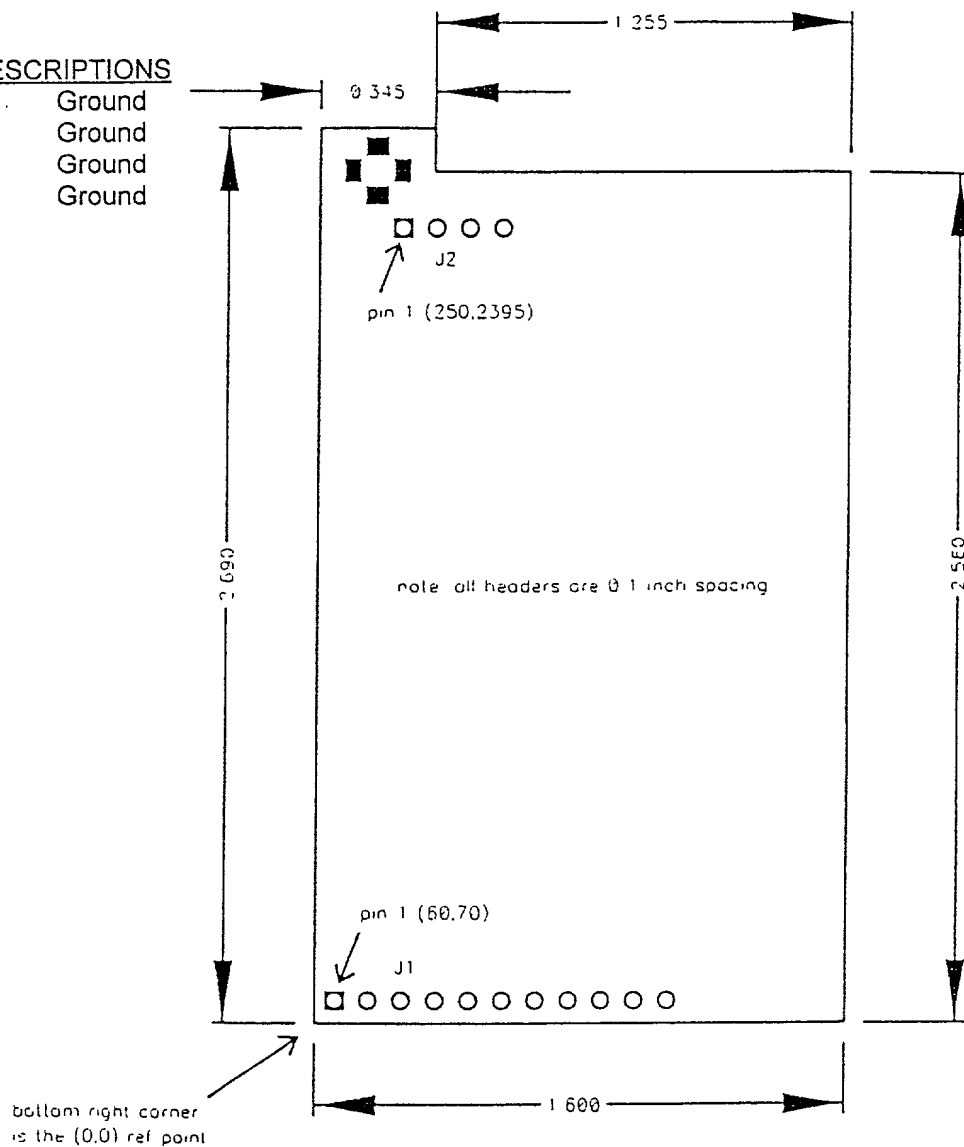


Fig. 4a

Pin	Signal	Type	Description
1	CTS	Output	Clear to send Flow control
2	PwrDn	Input	Power Down
3	RX	Output	Receive Data
4	TX	Input	Transmit Data
5	NC	-	Reserved
6	*Reset	Input	Reset radio (assert low to reset)
7-9	NC	-	Reserved
10	Vcc	Input	5 VDC, +/-0.3V
11	Gnd	-	Signal and chassis ground

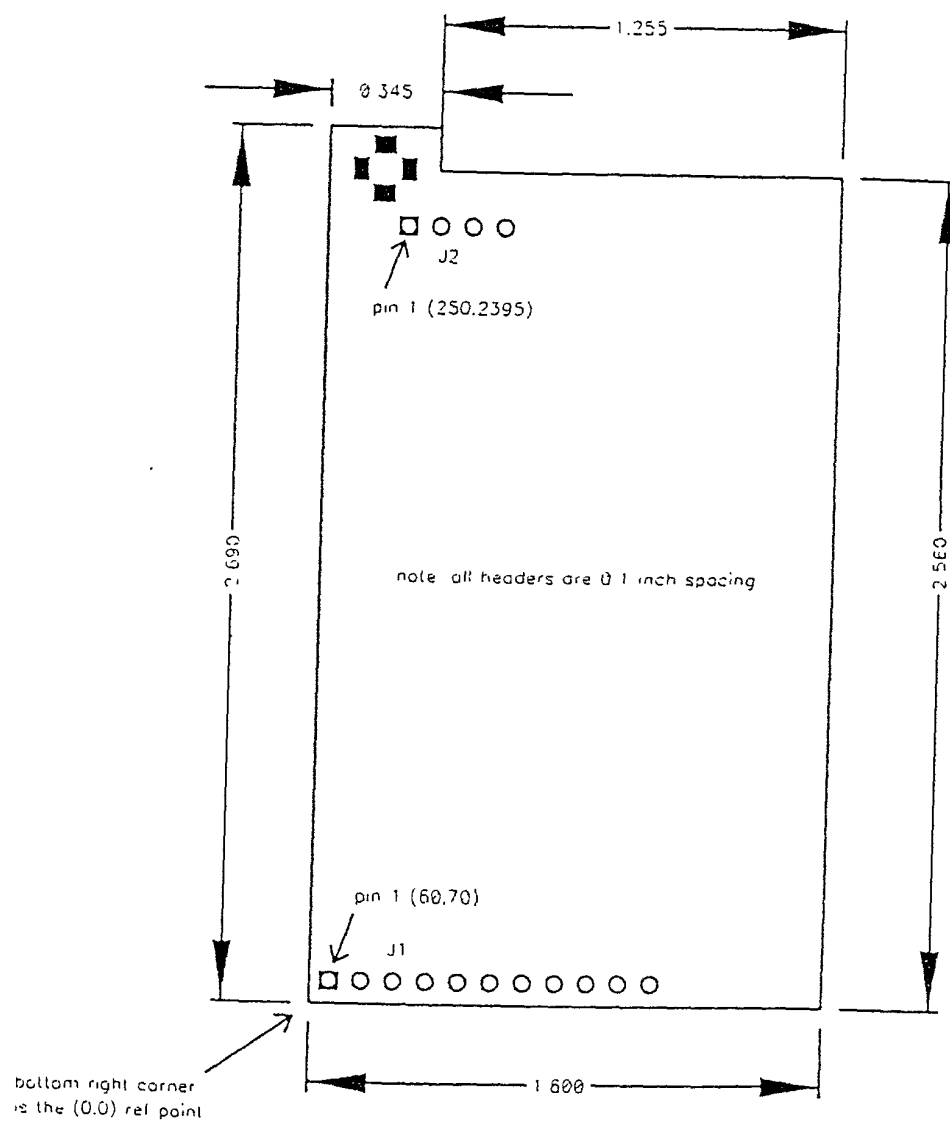


Fig. 4b

Pin	Signal	Type	Description
1	CTS	Output	Clear to send flow control
2	NC		Reserved
3	RX	Output	Received Data
4	TX	Input	Data to transmit
5	NC		Reserved
6	*RESET	Input	Reset (assert low to reset radio)
7	NC		Reserved
8	NC		Reserved
9	NC		Reserved
10	VCC	Input	+5 VDC +/-0.3V (200mA)
11	GND		Signal and chassis ground

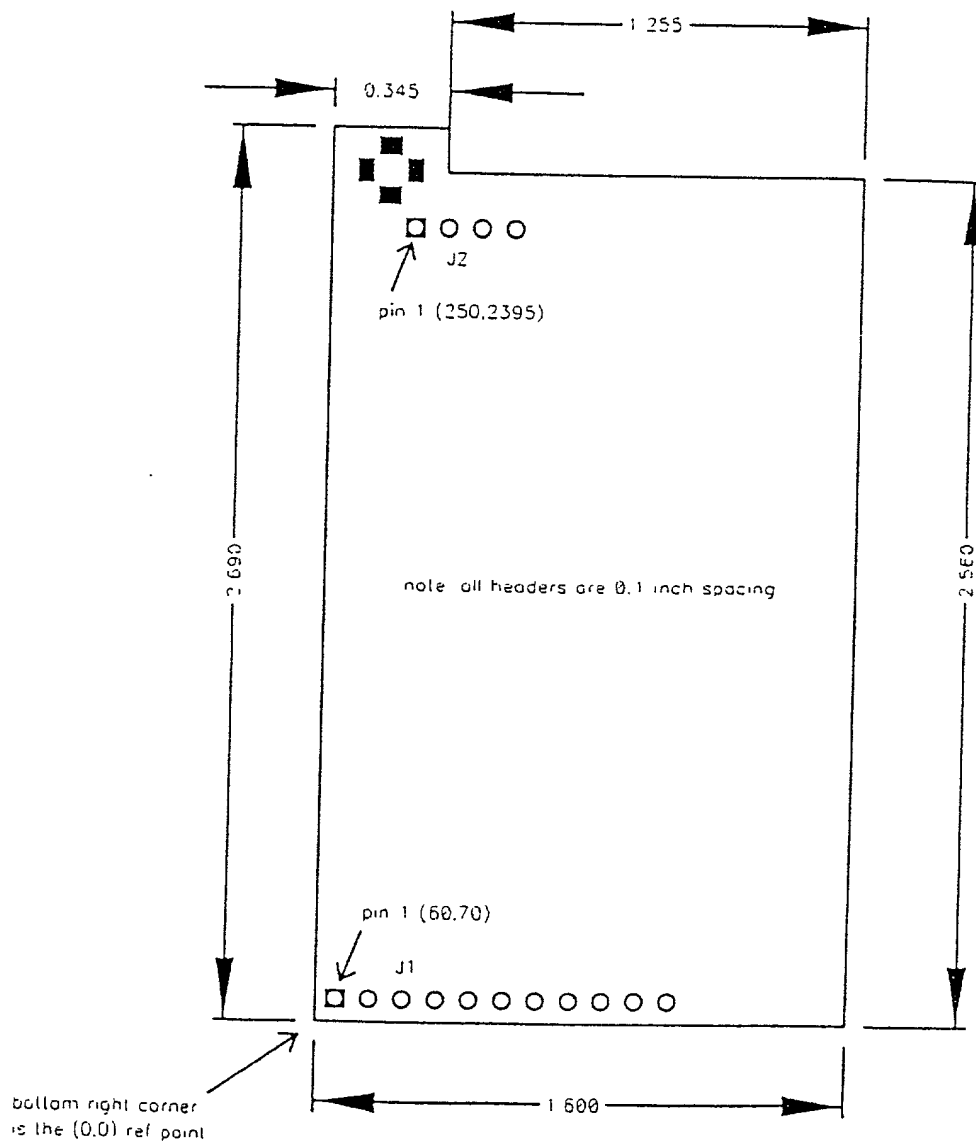
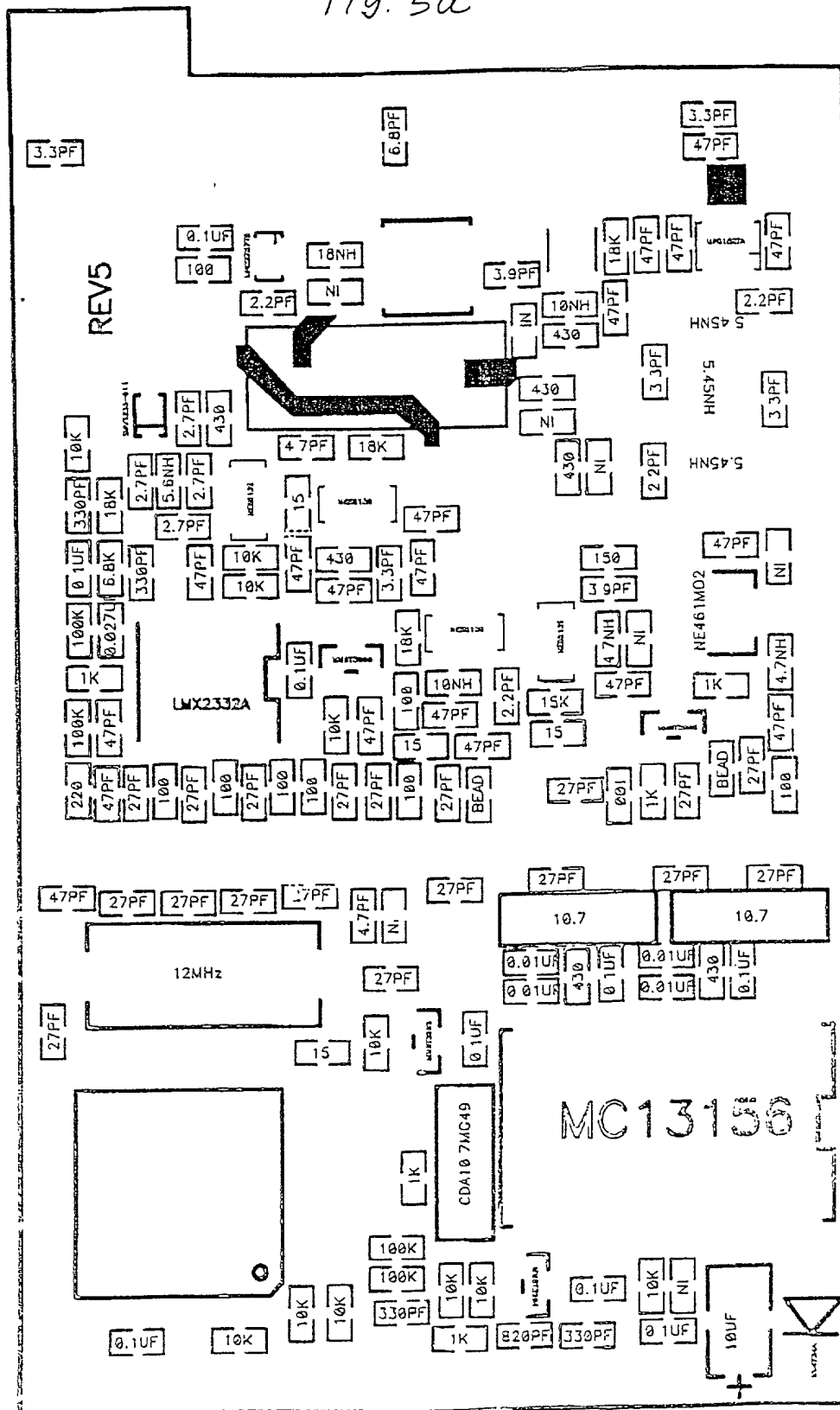


Fig. 4c

Fig. 5a



[illegible]

Fig. 5b

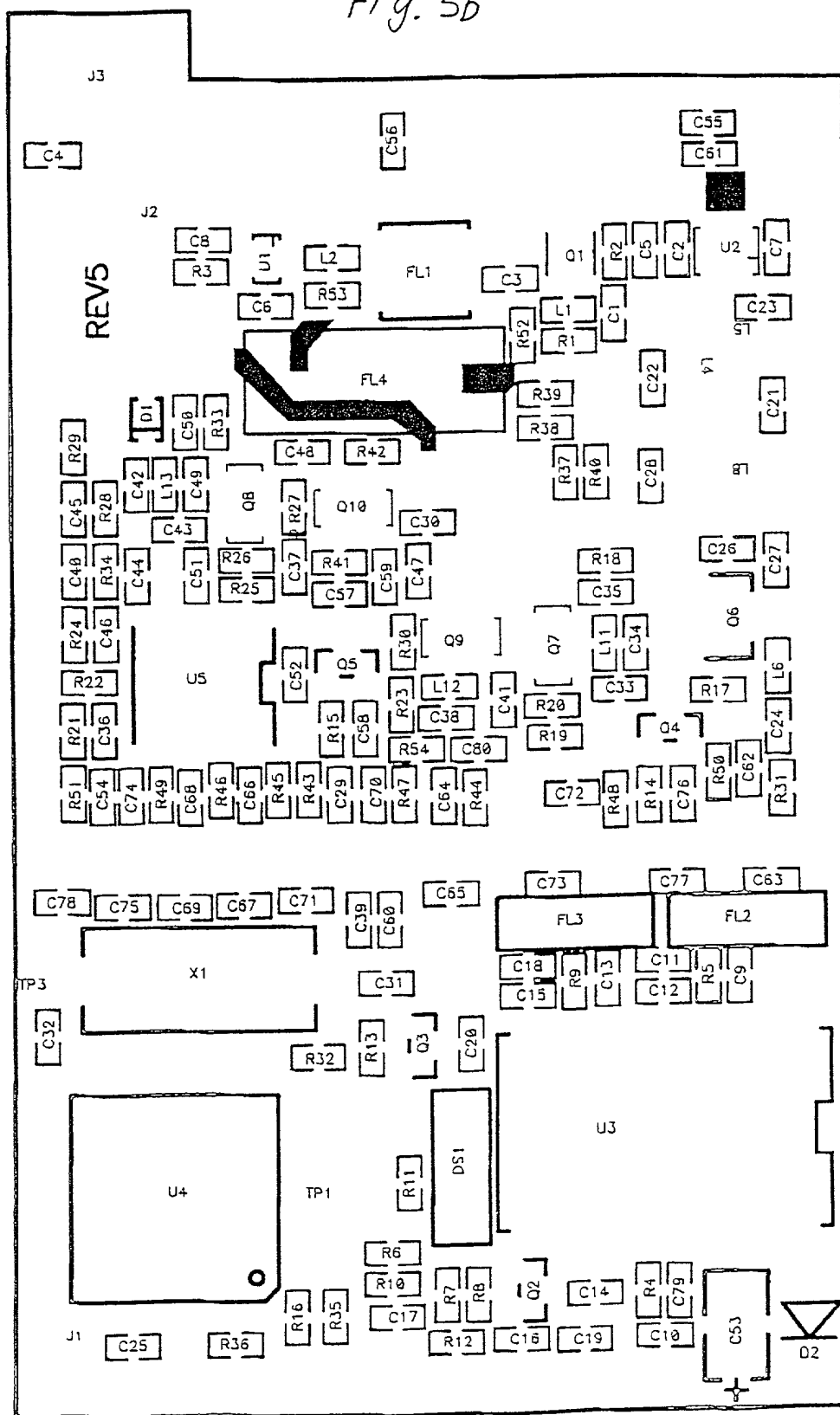


Fig. 5c

